UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,114	07/14/2003	Louis K. Scheffer	CA7035292001	9085

23639 7590 04/12/2005

BINGHAM, MCCUTCHEN LLP
THREE EMBARCADERO CENTER
18 FLOOR
SAN FRANCISCO, CA 94111-4067

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,114	SCHEFFER ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/2/04; 6/01/04; 6/24/04; 6/01/04 & 8/20/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1 and 13 are objected to:

the recitation of " the layer" is not clear to what applicants intend to mean.

2. In claim 20, line 1 delete "method", insert -- system--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-34 are rejected under 35 U.S.C. 102(b) as being unpatentable by Liebmann et al. (US Patent 5,740,068).

As to claims 1, 13, 25 and 30 Liebmann discloses:

(1) A method comprising:

generating an integrated circuit design (col.1, ll.23-26; col.3, ll.30-31);

creating a design database containing design data for each layer (level) of the design (col.1, ll.28-32; col.7, ll.1-7);

creating context information for features of a layer of the design (col.7, ll.32-50);

analyzing (the method illustrated in FIGS. 9 and 10 group the design shapes into three categories, with the first being those requiring proximity correction, the second

being those contributing to the proximity environment, and the third being those defining chip functionality) the context information to identify important attributes of features of the layer (col.6, ll.60-64; col.7, ll.51-67; col.8, ll.1-19);

partitioning (binning/bucketing) the layer into a plurality of stripes (col.5, ll.19-27);

assigning each feature to one or more of the plurality of stripes (sorting respective edge projections into buckets) based upon the importance of the attributes of the feature (col.5, ll.36-55; col.5, ll.66-67; col.6, ll.1-12); and

devising a writing plan to write each feature within the corresponding stripe (resizing sorted adage projections to create final proximity corrected feature) (col.5, ll.56-65; col.6, ll.13-40; col.8, ll.31-45);

(13) A system comprising:

means for generating an integrated circuit design (col.1, ll.23-26; col.3, ll.30-31);

creating a design database containing design data for each layer (level) of the design (col.1, ll.28-32; col.7, ll.1-7);

means for creating context information for features of a layer of the design (col.7, ll.32-50);

means for analyzing (the method illustrated in FIGS. 9 and 10 group the design shapes into three categories, with the first being those requiring proximity correction, the second being those contributing to the proximity environment, and the third being those defining chip functionality) the context information to identify important attributes of features of the layer (col.6, ll.60-64; col.7, ll.51-67; col.8, ll.1-19);

means for partitioning (binning/bucketing) the layer into a plurality of stripes (col.5, ll.19-27);

means for assigning each feature to one or more of the plurality of stripes (sorting respective edge projections into buckets) based upon the importance of the attributes of the feature (col.5, ll.36-55; col.5, ll.66-67; col.6, ll.1-12); and

means for devising a writing plan to write each feature within the corresponding stripe (resizing sorted adage projections to create final proximity corrected feature) (col.5, ll.56-65; col.6, ll.13-40; col.8, ll.31-45);

(25) A method comprising:

generating integrated circuit design data having a plurality of polygons (col.1, ll.23-26; col.3, ll.30-31);

determining context information from the integrated circuit design data (col.7, ll.32-50); and

analyzing features of the design data with the context information to distinguish important attributes of features from unimportant attributes and features (col.6, ll.60-64; col.7, ll.51-67; col.8, ll.1-19);

(30) A method comprising:

means for generating integrated circuit design data having a plurality of polygons (col.1, ll.23-26; col.3, ll.30-31);

means for determining context information from the integrated circuit design data (col.7, ll.32-50); and

means for analyzing features of the design data with the context information to distinguish important attributes of features from unimportant attributes and features (col.6, ll.60-64; col.7, ll.51-67; col.8, ll.1-19).

As to claims 2-12, 14-24, 26-29 and 31-33 Liebmann recites:

(2), (9), (14), (21), (28), (29), (33), (34) The method/system, wherein analyzing the context information to identify important features comprises identifying important attributes of the design and identifying polygons with the important attributes (col.6, ll.60-64; col.7, ll.51-67; col.8, ll.1-19);

(3), (15) The method/system, further comprising dividing each important polygon into a plurality of shapes and for each polygon, identifying shapes with important attributes (col.8, ll.46-65);

(4), (6), (16), (18) The method/system, wherein assigning each feature to one stripe, consistent with the attributes of each shape (col.5, ll.36-55; col.5, ll.66-67; col.6, ll.1-12);

(5), (17) The method/system, wherein analyzing the context information to identify important features comprises displaying the design data, context information for the features to the user and receiving an identification of the important attributes of features from the user (col.4, ll.50-67; col.6, ll.1-6);

(7), (8), (12), (19), (20), (23), (24) The method/system, further comprising calculating a writing time for the writing plan (col.8, ll.66-67; col.9, ll.1-5);

(10), (22) The method/system, wherein partitioning the layer into a plurality of stripes comprises automatically generating partitions so that each important feature is within one of the stripes (col.5, ll.19-27);

(26), (31) The method/system comprising adjusting a mask writing process (col.3, ll.24-29; col.5, ll.56-65; col.6, ll.13-40; col.8, ll.31-45);

The method/system, wherein context information for the design features comprises information for neighboring geometries, electrical intent of the features, and relationships of a given feature to neighboring features (col.7, ll.59-67; col.8, ll.1-19).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pang et al. (US Patent 6,578,188) describes mask defect printability simulation server that provides simulations, analysis, and reports to multiple clients over a wide area network. Multiple users can view the same mask defect image and provide real-time comments to each other as simulation and analysis are performed on the defect image, thereby encouraging problem solving and decision-making.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naum Levin

NL

Naum Levin

AV - 2825